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Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JANUARY 2017

Course Code: **EC 207**

Course Name: **LOGIC CIRCUIT DESIGN (AE, EC)**

Max. Marks: 100 Duration: 3 Hours

PART A **(2x15=30)**

(Answer two questions, Question no. 3 is compulsory)

1. a) Prepare a table for the first 12 integers in Binary, Grey, Excess 3 and ASCII. (4)

b) Perform the following operations [showing the intermediate steps]. (6)

i) $11000_2 - 10111_2$ using 1's and 2's complement method

ii) $7461_8 + 7157_8$

iii) $DC5A_{16} - 9B3C_{16}$

iv) 11001001101.1011011_2 into Decimal, Octal and Hexadecimal

c) What is Hamming code? How is the Hamming code word generated? The message "**1001001**" is coded in the 7-bit even parity Hamming code, which is transmitted through a noisy channel. Decode the message, assuming that at most a single error occurred in each code word. (5)

2. a) A four variable Boolean function is given as $F = A.B.C + A.\overline{C}.D + B.C.D$ where $A.B.\overline{C}.\overline{D} + A.\overline{B}.C.D + \overline{A}.\overline{B}.C.D$ are don't cares. Use Karnaugh map to find the minimal SOP expression for F. Design and realize the function F i) using NAND gates only and ii) using NOR gates only. (8)

b) Design and realize a combinational circuit to compare two 3 bit numbers A ($A_2A_1A_0$) and B ($B_2B_1B_0$) as inputs and "AGT"(A>B), "AEQ"(A=B) and "ALT"(A<B) are the outputs.[Use algorithmic approach]. (7)

3. a) Perform each of the following conversions [show the intermediate steps]. (8)

(i) 160.67_{10} into Hexadecimal (ii) $A63.B5_{16}$ into Decimal

(ii) ABBA into ASCII (iv) 12_{10} into BCD

(iii) 835_{10} into ASCII (vii) 28.3_{10} into Ternary(Radix 3)

(iv) 241.32_5 into Decimal (viii) -85_{10} into 2's complement

b) Draw the gate level circuit diagram and logic equations for a 1 to 4 de-multiplexer. For the Boolean function $\mathbf{F} = (A + B).(A + C).(B + C)$. Show how it can be implemented using a 1: 8 de-multiplexer and one or more gates. (7)

PART B (2x15=30)

(Answer two questions, Question no. 6 is compulsory)

4. **a)** Draw the circuit diagram of a transistor level CMOS NAND gate and explain the working with a truth table. (5)

   b) Define the terms noise margin, voltage and current levels, propagation delay, fan out and power dissipation related to a logic families. Prepare a comparison table showing the values of each for the TTL, ECL and CMOS logic families. (6)

   c) What is PLDs? Differentiate between PAL and PLA. (4)

5. **a)** Show how four 2-input NAND gates can be connected together to implement a clocked SR latch. Describe its operation with its detailed truth table; also derive its characteristic equation and excitation table.

   b) An up/down binary counter is required. There is one control input (**M**) and a clock (**CLK**). The outputs are to be labelled Q_0, Q_1 and Q_2. If **M**=1 then the counter counts up every clock period, if **M**=0 it counts down. Realize this counter in terms of AND, OR and XOR gates, and T flip flops. Provide equations for the inputs to the flip flops and a circuit diagram of the complete system.

6. **a)** Draw the circuit diagram of a transistor level TTL NOT gate and explain the working with a truth table. (4)

   b) Draw a circuit to control an LED via a TTL inverter for the following conditions: When the input to the inverter is 1, the LED should illuminate and the ON current should not exceed 15 mA, at which point the voltage drop across the LED will be 1.5V. Find the resistor values and justify your answer with sourcing and sinking mode of operation. (3)

   c) Design a circuit to obtain the sequence 2; 4; 3; 6; 2; 4; : : : using JK flip flops. (8)

PART C (2x20=40)

(Answer two questions, Question no. 9 is compulsory)

7. **a)** Draw the logic diagram of a four bit, parallel in serial out (PISO) shift register with LOAD/$\overline{SHIFT}$ control and explain its working. (10)

   b) Draw the state diagram, transition table, D flip flop excitation table and state equation for the given state table. (10)

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
A (00)	A	B	0	0
B (01)	C	B	0	0
C (10)	A	D	0	0
D (11)	C	B	1	0

8. A serial data line carries binary data to a system with input **X**. The system is required to detect a sequence 0 1 0 in the data and give an output **Y** = 1 at the end of the sequence. Only non-overlapping sequences should be detected in the data. For example, the output y should only be 1 for the 0 underlined in the input sequence : : : 1 0 1 **0** 1 0 1 **0** : : :.

Draw the state diagram, state table, transition table, excitation table for the Mealy clocked synchronous sequential system and realize it with minimum number of D-flip flops after state reduction, if possible. (20)

9. **a)** Draw the logic diagram of a four bit ring counter and explain the working with truth table and timing diagram. (10)

b) Minimize the state table using implication chart. The state machine is having nine states, one input and two output variables. Re-assign the simplified state variables as A, B, C, D and E. (10)

Present state	Next state		Output (Z_1Z_2)	
	X=0	X=1	X=0	X=1
0	0	1	00	00
1	4	2	00	00
2	7	1	00	00
3	2	6	01	10
4	6	5	10	00
5	3	4	01	11
6	1	6	01	10
7	3	8	10	00
8	8	7	01	11