Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code: **EC 207**

Course Name: **LOGIC CIRCUIT DESIGN (AE, EC)**

Max. Marks: 100 Duration: 3 Hours

PART A

Answer two questions, Question no. 3 is compulsory.

1. **a)** Convert the first twelve integers into Binary, Grey and BCD. (4)

   b) Perform the following operations [show the intermediate steps]. (6)

   i) $5743)_8 - 3672)_8$

   ii) $CFD4)_{16} - 6A51)_{16}$

   iii) $56)_{10} - 48)_{10}$ using 2's and 1's complement method

   iv) $316.645)_{10}$ into Binary, Octal and Hexadecimal

   c) What is Hamming code? How is the Hamming code word tested and corrected. Encode the data bits "**1101**" into the 7-bit even parity Hamming code. (5)

2. **a)** Show how four single bit full adders can be combined to implement a four bit ripple carry adder. Design and realize a four bit adder/subtract circuit using the four bit adder block and logic gates. The $\overline{add/subtract}$ function can be selected by using a control signal. Justify your answer with at least one example from each category. (5)

   b) For the Boolean function $F = \bar{A}.\bar{B}.\bar{C} + A.\bar{C}.\bar{D} + \bar{A}.C.D + B.C.\bar{D} + \bar{B}.C.D$. Show how it can be implemented using **i)** One 16:1 multiplexer **ii)** One 8:1 multiplexer and one or more NOT gates. (10)

3. **a)** In a computer system, numbers are represented using words with a length of 4 bits.

   (i) What is the range of positive numbers that can be represented using unsigned binary numbers?

   (ii) Explain how the 1's and 2's complement representation can be used to describe signed binary numbers.

   (iii) Prepare a table showing all the positive and negative numbers which can be represented using 4 bit words in "sign magnitude", "1's complement" and "2's complement" representation and mark the maximum and minimum in each case. (8)

   b) Design and realize a 8:3 priority encoder. (7)

PART B

Answer two questions, Question no. 6 is compulsory.

4. **a)** Define the terms noise margin, voltage and current levels, propagation delay, fan out and power dissipation related to a logic families. Prepare a comparison table showing the values of each for the TTL, ECL and CMOS logic families. (6)

b) Draw the circuit diagram of a transistor level TTL NAND gate and explain the working. (5)

c) What is PLDs?. Differentiate between PAL and PLA. (4)

5. a) Realize a JK flip flop with NAND gates and describe its operation with detailed truth table, characteristic equation and excitation table. Describe the race around problem and suggest the methods to eliminate. (5)

b) A self starting synchronous binary up-counter having the state sequence 1; 2; 3; 4; 5; 6; 1; 2; : : : is to be implemented using T-flip flops. The flip flop outputs are designated as Q_2, Q_1 and Q_0, where Q_0 represents the least significant digit of the count. Give simplified expressions for the required next-state logic and the complete circuit diagram. (10)

6. a) Draw the circuit diagram of a transistor level CMOS NOR gate and explain the working with a truth table. (4)

b) Differentiate between the totem pole, open collector and tri-state logic related to the TTL logic circuit. (3)

c) Describe the procedure for converting one type of flip flop in to another. Perform the following conversions. (8)

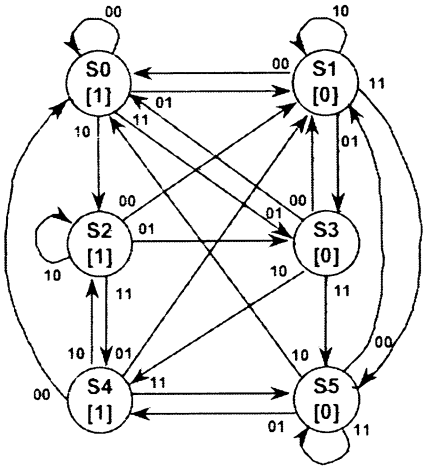
i) T to JK ii) T to D

PART C

Answer two questions, Question no. 9 is compulsory.

7. a) Draw the logic diagram of a four bit Johnson counter and explain the working with truth table and timing diagram. (10)

b) Obtain the state table, transition table and D flip flop excitation table for the state diagram shown in figure. (10)



8. Draw the state diagram, state table, transition table, excitation table for the Mealy clocked synchronous sequential system (modulo-4 up/down counter). Design and realize it with minimum number of T-flip flops. The system has two control inputs

and two outputs: input (mode) **M** is set at logic "**0**" to cause the counter to count up, and at logic "**1**" to cause the counter to count down; input (enable) **E** is set at logic "**1**" to enable the counter to count and at logic "**0**" to cause the counter to hold its current state. The outputs "Y,Z" become "00", "01", "10",and "11" in count up direction and output "Y,Z" become "11", "10", "01",and "00" in countdown direction against the clock starting from the first state. (20)

9. **a)** Draw the logic diagram of a four bit, bi-directional serial in serial out (SISO) shift register with mode control and explain the working with timing diagram. (10)

b) Reduce the state table and identify the redundant states. (10)

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
S_0	S_1	S_2	0	0
S_1	S_3	S_4	0	0
S_2	S_5	S_6	0	0
S_3	S_7	S_8	0	0
S_4	S_9	S_{10}	0	0
S_5	S_{11}	S_{12}	0	0
S_6	S_{13}	S_{14}	0	0
S_7	S_0	S_0	0	0
S_8	S_0	S_0	0	0
S_9	S_0	S_0	0	0
S_{10}	S_0	S_0	1	0
S_{11}	S_0	S_0	0	0
S_{12}	S_0	S_0	1	0
S_{13}	S_0	S_0	0	0
S_{14}	S_0	S_0	0	0

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