Course code	Course Name	L-T-P - Credits	Year of Introduction
CS369	Digital System Testing & Testable Design	3-0-0-3	2016

Pre-requisites : **CS234** Digital Systems Lab

Course Objectives

- To expose the students to the basics of digital testing techniques applied to VLSI circuits.
- To introduce the concepts of algorithm development for automatic test pattern generation for digital circuits.
- To discuss fundamentals of design for testability.

Syllabus

Basic terminology used in testing - functional and structural models of digital systems -logic simulation for design verification and testing-fault modeling - fault simulation - testing for faults - design for testability.

Expected Outcome

The students will be able to

i. Appreciate the basics of VLSI testing and functions modeling of circuits.
ii. Apply fault modeling using single stuck & multiple stuck modeling for combinational circuits.
iii. Evaluate different methods for logic and fault simulations.
iv. Generate test patterns using automatic test pattern generation methods like D, PODEM & FAN algorithms for combinational circuits.
v. Explain automatic test pattern generation using time frame expansion and simulation based method for sequential circuits.
vi. Design digital circuits using scan path and self tests.

Text Books

1. Alexander Miczo, Digital Logic Testing and Simulation, Wiley, 2e, 2003.
2. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2002.
3. Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishers, 2006.

Reference

1. Zainalabedin Navabi, Digital System test and testable design, Springer, 2011.

Course Plan

Module	Contents	Hours	End Sem. Exam Marks
I	**Fundamentals of Testing:** Testing & Diagnosis, testing at different levels of abstraction, errors & faults, modeling & evaluation,types of testing, test generation **Modeling:** Functional modeling at logic level, functional modeling at register level & structural models.	06	15%
II	**Fault Modeling :** Logic fault models, Fault detection and redundancy, Fault equivalence & fault location, fault dominance, single stuck faults, multiple stuck fault models .	06	15%
FIRST INTERNAL EXAM			

III	**Logic & fault Simulation:** Simulationfor verification& test evaluation, types of simulation – compiled code & Event driven, serial fault simulation, statistical method for fault simulation.	**07**	**15%**
IV	**Combinational circuit test generation**: ATG for SSFs in combinational circuits – fault oriented ATG- fault independent ATG- random test generation, Sensitized path, D-algorithm, PODEM and FAN.	**07**	**15%**
SECOND INTERNAL EXAM			
V	**Sequential circuit test generation:** ATPG for single clock synchronous circuits, time frame expansion method, simulation based sequential circuit ATPG – genetic algorithm.	**07**	**20%**
VI	**Design for Testability:** introduction to testability, design for testability techniques, controllability and observability by means of scan registers, generic scan based designs – scan path, boundary scan, Introduction to BIST**.**	**09**	**20%**
END SEMESTER EXAM			

Question Paper Pattern:

1. There will be *five* parts in the question paper – A, B, C, D, E
2. Part A
    a. Total marks : 12
    b. *Four*questions each having *3* marks, uniformly covering modules I and II;All*four* questions have to be answered.
3. Part B
    a. Total marks : 18
    b. *Three* questions each having *9* marks, uniformly covering modules I and II; *Two* questions have to be answered. Each question can have a maximum of three sub-parts
4. Part C
    a. Total marks : 12
    b. *Four* questions each having *3* marks, uniformly covering modules III and IV; All*four* questions have to be answered.
5. Part D
    a. Total marks : 18
    b. *Three* questionseach having *9* marks, uniformly covering modules III and IV; *Two* questions have to be answered. Each question can have a maximum of three subparts
6. Part E
    a. Total Marks: 40
    b. *Six* questions each carrying 10 marks, uniformly covering modules V and VI; *four* questions have to be answered.
    c. A question can have a maximum of three sub-parts.
7. There should be at least 60% analytical/numerical/design questions.