C B3C045 **Total Pages:4**

Reg. No. _____ Name _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JANUARY 2017

Course Code: **EE 203**

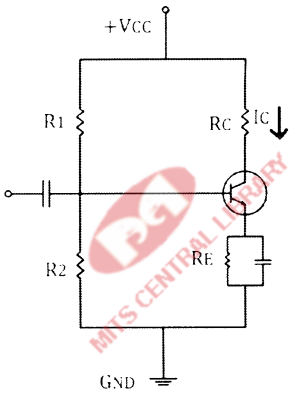
Course Name: **ANALOG ELECTRONIC CIRCUITS (EE)**

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 5 marks.

1. Draw the dc and ac load lines for the transistor circuit. Given R_1=18KΩ, R_2=8.2KΩ, R_C=2.2KΩ, V_{cc} =20V, R_E=2.7KΩ.



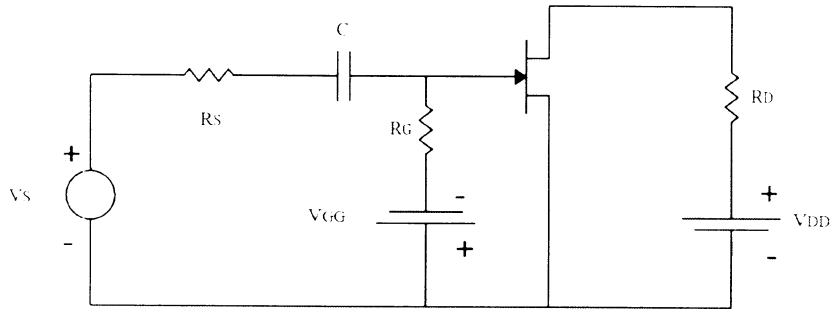
2. Why does gain of amplifier falls off at low and high frequencies?
3. List the characteristics of an amplifier that get modified by negative feedback.
4. a) What are the modes in which an op-amp can be operated?

   b) An op-amp has a gain bandwidth product of 15 MHz. Determine the bandwidth of op-amp when A_{CL} =500. Also find maximum value of A_{CL} when frequency is 200 KHz.
5. Design an adder circuit to get the output expression as $V_o = -[0.1\ V_1 + V_2 + 10\ V_3]$ where V_1, V_2 and V_3 are the inputs to the Op-amps.
6. What are the limitations of an ideal integrator? Design a circuit which overcome the errors of ideal integrator.
7. Distinguish between triangular wave and ramp generator using op-amp.
8. Design a phase shift oscillator with a frequency of 100 Hz using op-amp.

PART B

Answer any 2 questions. Each question carries 10 marks.

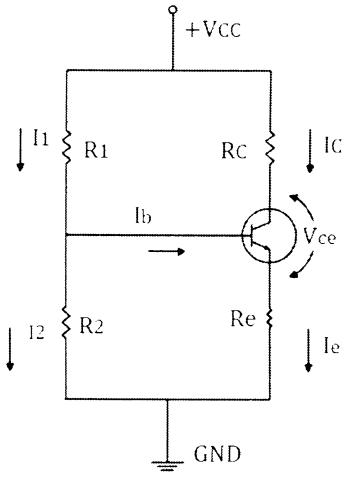
9. a) Parameters of FET used in amplifier circuits are g_m=4.2 m℧ and r_d=30KΩ. Assume C to be short circuit for signal frequency, given a small signal model for the amplifier. Determine small signal voltage gain if R_D =6.8KΩ, R_G = 1MΩ and R_S=10 KΩ.



(2.5)

b) Compare JFET with MOSFET. (2.5)

c) Why is voltage divider bias relatively stable against changes in h_{fe}? ii) Design voltage divider bias circuit to operate from a 12V supply. The bias conditions are V_{CE}=3V, V_E=5V and I_c=1mA. (5)



10. a) A transistor used in CE connection has the following set of h parameters when the d.c. operating point is V_{CE} =5V and I_C = 1 mA; h_{ie} =1700 Ω ; h_{re} =1.3 ×10-4; h_{fe} = 38; h_{oe} = 6 × 10 $^{-6}$ ℧. If the a.c. load r_L seen by the transistor is 2 KΩ . find (i) the input impedance (ii) current gain (iii) voltage gain (5)

b) Why the gate junction of FET is always reverse biased? List the parameters of JFET from characteristics. (5)

11. a) Explain any compensation technique adopted in transistor amplifier for reducing the drift of operating point. (5)

b) The datasheet of an N-channel JFET gives the following details I_{Dss} = 9 mA and pinch off voltage of -4.5V i) At what value of V_{GS} will I_D be equal to 3 mA?
ii) What is its g_m at this I_D? (5)

PART C

Answer any 2 questions. Each question carries 10 marks.

12. a) A differential amplifier has inputs V_{S1} =10mV and V_{S2}= 9mV. It has differential mode gain of 60 dB and a CMRR of 80 dB. Find the percentage error in output and error voltage. (2)

b) State the Barkhausen criterion for sinusoidal oscillators and why this must be fulfilled to sustain oscillations? (3)

c) For a class B power amplifier using a supply of Vcc =12V and driving a load of 8Ω. Determine maximum load power. DC input power and collector efficiency. (5)

13. a) An amplifier with negative feedback has a voltage gain of 100. It is found that without feedback an input signal of 50mV is required to produce a given output, whereas with feedback, the input signal must be 0.6V for same output. Calculate the value of A and β. (5)

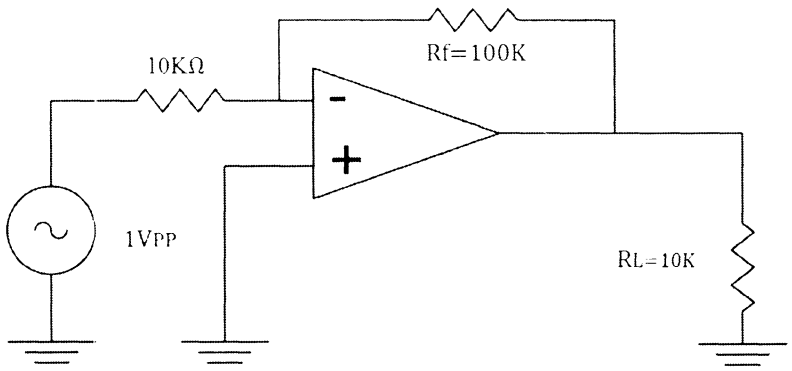
b) Show how piezo-electric crystals are employed for oscillator stabilization. (3)

c) A crystal has the following parameters L = 0.33H,C_1 = 0.065pF,C_2 = 1.0pF and R=5.5KΩ. Determine series resonant frequency and Q factor of the crystal. (2)

14. a) Compare the merits and demerits of different types of inter stage coupling in amplifiers (3)

b) What is cross over distortion? Why most power amplifiers used in practice are designed to operate in class AB stage? (2)

c) An inverting op-amp with slew rate 0.5V/μsec is shown in the figure. Determine i) closed loop voltage gain ii) input impedance of the circuit iii) Maximum operating frequency



(5)

PART D

Answer any 2 questions. Each question carries 10 marks.

15. a) Draw the circuit diagram of an astable-multivibrator using 555 timer to generate the output signal with frequency 2 KHz and duty cycle of 75 %. (5)

    b) What are the advantages and features of instrumentation amplifier? Derive the expression for output voltage of instrumentation amplifier. (5)

16. a) Design a Wein bridge oscillator circuit to produce a 100KHz. ± 9Voutput. Design amplifier to have closed loop gain of 3. (5)

    b) What is the function of precision rectifier circuits? What is the significance of UTP and LTP in Schmitt trigger circuits? (5)

17. a) Discuss how logarithmic amplifier is realized with op-amp circuitry. (5)

    b) What is the basic principle of RC oscillators? Design a phase shift oscillator to oscillate at 500Hz. (5)

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